AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S MAIN BRIEF ON APPEAL

APPELLANT:	Tohisharu Yanagida	OLD DOCKET NO.:	P99,1318
		NEW DOCKET NO.:	09792909-4298
SERIAL NO.:	09/385,959	GROUP ART UNIT:	2822
DATE FILED:	August 30, 1999	EXAMINER:	D. Graybill
INVENTION:	"SEMICONDUCTOR APPARATUS AND PROCESS OF PRODUCTION THEREOF"		

Mail Stop Appeal Brief - Patents
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Appellant submits herewith Appellant's Main Brief on Appeal under 37 C.F.R. §41.37 in support of the Notice of Appeal mailed on December 5, 2005. The Commissioner is hereby authorized to charge the amount of $500.00 for the requisite filing fee for filing the Main Brief on Appeal to the Appellants' Attorneys' credit card. Form 2038 is attached.

Appellant petitions the Commissioner of Patents and Trademarks to extend the time for filing this brief for two months so that the period for filing is extended to April 5, 2006. Postal money order no. 05457230278 in the total amount of $450.00 is enclosed for the two-month extension fee.

The Commissioner is hereby authorized to charge any deficiency in fees associated with this communication or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

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Respectfully Submitted,

 (Reg. No. 45,034)

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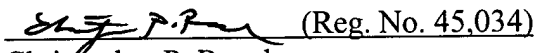
CERTIFICATE OF MAILING

I hereby certify that correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 5, 2006.

 (Reg. No. 45,034)

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P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. §41.37, Appellant submits this Main Brief on Appeal pursuant to the Notice of Appeal filed on December 5, 2005 in the above-identified application.

I. REAL PARTY IN INTEREST:

The real party in interest in the present appeal is the Assignee, Sony Corporation. The assignment was recorded in the U.S. Patent and Trademark Office at Reel 010378, Frame 0094.

II. RELATED APPEALS AND INTERFERENCES:

Appellant is not aware of any related appeals or interferences.

III. STATUS OF CLAIMS:

Claims 1-8 and 10-21 are pending in the application. Claims 1-6 have been withdrawn from consideration as being directed to a non-elected invention.

The present appeal is directed to claims 7, 8 and 10-21, which were finally rejected in an Office Action dated August 4, 2005. A copy of claims 7, 8, and 10-21 is appended hereto as the Claims Appendix.

The status of the claims on appeal is as follows:

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Claims 7, 8, 10, 11, 16, and 19-21 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Hayes (U.S. Patent No. 6,114,187)("Hayes")* in view of *Hotchkiss (U.S. Application No. 2002/0106832)("Hotchkiss")* and *Behun (U.S. Patent No. 5,147,084)("Behun")*.

Claims 12, 13, and 17 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Hayes , Hotchkiss* and *Behun*, and further in view of *Nishikawa, et al. ("U.S. Patent No. 6,227,436")("Nishikawa")* and *Denning, et al. ("U.S. Patent No. 6,187,682")("Denning")*.

Claims 14 and 15 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Hayes, Hotchkiss, Behun, Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura ("U.S. Patent No. 4,807,021")("Okumura")*.

Claim 18 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss* and *Behun*, and further in view of *Jackson ("U.S. Patent No. 5,068,040")("Jackson")*.

IV. STATUS OF AMENDMENTS:

All amendments have been entered in this application.

V. SUMMARY OF CLAIMED SUBJECT MATTER:

The claimed invention relates to a method of producing a semiconductor apparatus.

As described in Appellant's specification, the claimed method enables the thermal stress between a semiconductor device and a mounting board to be relieved without the use of a sealing resin. Further, the claimed method reduces the resistance of the connection between the semiconductor device and the mounting board and increases the strength of the connection. (Specification, page 9, lines 10-16).

Referring to Applicant's Figures 4 and 5 as an illustrative example, Appellant's independent claim 7 claims a method of producing a semiconductor apparatus by forming metal ball bumps 116b in direct contact with a circuit pattern 114 of a semiconductor device formed on a semiconductor substrate 110 in a semiconductor wafer state. (Figure 4A; Specification, page

26, line 19-page 27, line 4). A resin film 117 is formed on a circuit pattern forming surface of the semiconductor device so as to seal spaces between said metal ball bumps 116b and to become thinner than a height of the metal ball bumps 116b. (Figure 4B; Specification, page 27, lines 5-19).

The surfaces of the metal ball bumps 116b projecting out from the resin film 117 are cleaned. (Figure 4C; Specification, page 27, lines 20-page 28, line 6). After the cleaning step, eutectic solder layers 118 that are different in composition from the metal ball bumps 116b are formed on the surfaces of the metal ball bumps 116b. (Figure 5A; Specification, page 28, lines 7-14). After the forming the solder layers 118 step, the semiconductor substrate is cut into unit semiconductor chips, each semiconductor chip having at least one of the semiconductor device. (Specification, page 28, lines 15-18).

After the cutting step, at least one of the semiconductor chips 100 is mounted on a mounting board 200 from a bump 116b forming surface side of the semiconductor chip so as to connect the eutectic solder layers 118 of the semiconductor chip 100 to the mounting board 200 with the resin film 117 directly contacting the semiconductor chip and not directly contacting the mounting board 200. (Figure 1 and 5B; Specification, page 29, line 8-page 30, line 15).

Thus, as shown in Applicant's Figure 5B, the eutectic solder layers 118 are formed on the metal ball bumps 116b. As shown in Figure 1, the resin film 117 does not directly contact the mounting board 200.

Claims 8 and 10-21 depend from claim 7.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL:

A. Claims 7, 8, 10, 11, 16, and 19-21 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Hayes (U.S. Patent No. 6,114,187)("Hayes")* in view of *Hotchkiss (U.S. Application No. 2002/0106832)("Hotchkiss")* and *Behun (U.S. Patent No. 5,147,084)("Behun")*.

B. Claims 12, 13, and 17 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Nishikawa, et al. ("U.S. Patent No. 6,227,436")("Nishikawa")* and *Denning, et al. ("U.S. Patent No. 6,187,682")("Denning")*.

C. Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Hayes*, *Hotchkiss*, *Behun*, *Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura ("U.S. Patent No. 4,807,021")("Okumura")*.

D. Claim 18 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Jackson ("U.S. Patent No. 5,068,040")("Jackson")*.

VII. ARGUMENT:

Claims 7, 8, and 10-21 stand rejected under 35 U.S.C. §103 by the Examiner as being unpatentable based on various references. As set forth more clearly below, the rejections of the claims set forth by the Examiner under §103 are improper and accordingly the Board should reverse these rejections.

A. Claims 7, 8, 10, 11, 16, and 19-21 are not unpatentable under 35 U.S.C. §103(a) based on the teachings of *Hayes* in view of *Hotchkiss* and *Behun*

Appellant respectfully submits that the Examiner's assertions are incorrect as a matter of fact and law. Thus, for the reasons set forth below, Appellant respectfully requests that this Board reverse the rejection of claims 7, 8, 10, 11, 16, and 19-21 under 35 U.S.C. §103(a) as being allegedly unpatentable based on the teachings of *Hayes* in view of *Hotchkiss* and *Behun*.

None of *Hayes*, *Hotchkiss* or *Behun*, taken singly or in combination, disclose or suggest metal ball bumps formed in direct contact with a circuit pattern, with eutectic solder layers formed on the surfaces of the metal ball bumps. Referring to *Hayes* Figure 2, *Hayes* discloses solder columns 3 formed in direct contact with a circuit pattern. *Hayes's* solder columns protrude

from a dielectric layer 4 and metal ball bumps 9 are formed on top of its solder columns 9 and dielectric layer 4, with no eutectic solder layers formed on its metal ball bumps 9. Thus, unlike Appellant's claimed invention, *Hayes* fails to disclose forming eutectic solder layers on metal ball bumps. Further, *Hayes* fails to teach forming metal ball bumps in direct contact with a circuit pattern. Instead, *Hayes* forms solder columns in direct contact with a circuit patter and forms metal ball bumps on the solder columns.

The Examiner proposes that Appellant admits that *Hayes* discloses metal ball bumps. *Office Action of 8/4/2005*, page 3. *Hayes* does disclose metal ball bumps, however as discussed above, *Hayes* fails to teach forming metal ball bumps in direct contact with a circuit pattern. *Hayes* Figure 7d clearly shows that *Hayes* forms metal ball bumps in direct contact with a solder column.

Referring to *Hotchkiss* Figure 13, *Hotchkiss* discloses metal ball bumps 114 that are formed in direct contact with a circuit pattern, but with no eutectic solder layers formed thereon. The "tops" of *Hotchkiss's* metal ball bumps 114 directly contact opposing metal pads 412 of an adjacent circuit board. Unlike Appellant's claimed invention, *Hotchkiss* fails to teach eutectic solder layers formed on its metal ball bumps 114. Accordingly, *Hotchkiss's* connection would suffer from reduced strength, less favorable resistance, and heat stress.

Referring to *Behun* Figure 1A, *Behun* teaches forming metal ball bumps 18 on LMP solder 16. This is similar to *Hayes*, which forms metal ball bumps on solder columns. Thus, like *Hayes, Behun* also fails to disclose forming metal ball bumps in direct contact with a circuit pattern and also fails to disclose forming eutectic solder layers on its metal ball bumps.

Therefore, none of the cited references, taken individually, teaches eutectic solder layers formed on metal ball bumps.

The Examiner argues that one having skill in the art allegedly would have been motivated to replace *Hayes's* solder columns with *Hotchkiss'* metal ball bumps to allegedly arrive at the

claimed invention. The Examiner argues that both *Hayes's* solder columns and *Hotchkiss'* metal ball bumps provide a conductive path and, therefore, one skilled in the art would have been motivated by *Hayes* in view of *Hotchkiss* to interchange *Hayes's* solder columns with *Hotchkiss'* metal ball bumps. Applicants respectfully disagrees.

Hayes clearly states that it uses solder columns instead of solder ball bumps to avoid accidentally short-circuiting its underlying electrical pads (*Hayes*, col. 9, line 62 - col. 10, line 9). Therefore, *Hayes* specifically teaches away from forming metal ball bumps on its electrical pads, and teaches to instead use solder columns. Therefore, *Hayes* in view of *Hotchkiss* would not teach one skilled in the art to replace *Hayes's* solder columns with *Hotchkiss'* solder ball bumps, since *Hayes* clearly teaches away from using solder ball bumps instead of solder columns. Therefore, *Hayes* in view of *Hotchkiss* fails to disclose or suggest claim 7.

Further, *Hayes* teaches using solder columns 3 as conductive paths through its dielectric layer 4, so that *Hayes's* metal ball bumps 9 can be electrically coupled to the underlying chip via the solder columns 3. *Hayes's* solder columns 3 are formed to serve as narrow vias in *Hayes's* dielectric layer 4. (*See, Hayes* Figure 7d). This is unlike *Hotchkiss's* metal ball bumps 114, which serve to solder-connect one device to another device. Therefore, Applicant respectfully submits that *Hayes's* solder columns 3 do not serve the same purpose as *Hotchkiss's* metal ball bumps 114. *Hayes's* solder columns 3 serve as vias, and *Hotchkiss's* metal ball bumps serve as direct solder-connects.

Nowhere do any of the cited references, taken singly or in combination, disclose or suggest forming eutectic solder layers on the surfaces of any metal ball bumps. *Hayes* discloses metal ball bumps 9 on its solder columns, but fails to disclose or suggest forming eutectic solder layers thereon. *Hotchkiss* discloses metal ball bumps 114 with no eutectic solder layers formed thereon. *Behun* discloses an LMP solder 16 having a HMP metal ball bump 18 formed thereon.

Therefore, unlike Applicant's claim 7, none of the cited references, taken alone or in combination, disclose or suggest a metal ball bump having a solder layer formed thereon. Accordingly, *Hayes* in view of *Hotchkiss* and *Behun* fails to disclose or suggest claim 7.

Claims 8, 10, 11, 16, and 19-21 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Appellants respectfully request that the Board reverse the rejection.

B. **Claims 12, 13, and 17 are not unpatentable under 35 U.S.C. §103(a) based on the teachings of *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Nishikawa, et al.* and *Denning, et al.***

Appellant respectfully submits that the Examiner's assertions are incorrect as a matter of fact and law. Thus, for the reasons set forth below, Appellant respectfully requests that this Board reverse the rejection of claims 12, 13, and 17 under 35 U.S.C. §103(a) as being allegedly unpatentable based on the teachings of *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Nishikawa, et al.* and *Denning, et al.*

As discussed above, *Hayes* in view of *Hotchkiss* and *Behun* fails to disclose or suggest Appellant's claimed method that includes forming a metal ball bump having a eutectic layer formed thereon, with the eutectic layer mounted to a mounting board.

Referring to *Nishikawa* Figure 1a and 1b, *Nishikawa* teaches that a flux or flux-containing cream 4 can be used to remove oxide film from a metal ball bump surface 2. However, *Nishikawa* teaches away from using flux or a flux-containing cream 4 because its use causes voids 5 in the metal ball bump 2. *Nishikawa* 1:31-40, Figure 1c. Accordingly, *Nishikawa* teaches removing residue 6 from a metal ball bump 2 using sputtering 7 prior to attaching the metal ball bump 2 to another surface. *Nishikawa* Figures 3 and 4.

Unlike Appellant's claimed invention, nowhere does *Nishikawa* disclose or suggest forming a eutectic solder layer on a metal ball bump. Instead, *Nishikawa* specifically teaches cleaning the surface of a metal ball bump so that it can be attached to another metal contact.

Denning fails to even discuss metal ball bumps or eutectic solder layers formed on metal ball bumps.

Therefore, *Hayes, Hotchkiss* and *Behun*, and further in view of *Nishikawa* and *Denning* still fails to disclose or suggest Applicant's claim 7.

Claims 12, 13 and 17 depend directly or indirectly from claim 7 and are therefore

allowable for at least the same reasons that claim 7 is allowable.

Appellants respectfully request that the Board reverse the rejection.

C. **Claims 14 and 15 are not unpatentable under 35 U.S.C. §103(a) based on the teachings of *Hayes, Hotchkiss, Behun, Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura***

Appellant respectfully submits that the Examiner's assertions are incorrect as a matter of fact and law. Thus, for the reasons set forth below, Appellant respectfully requests that this Board reverse the rejection of claims 14 and 15 under 35 U.S.C. §103(a) as being allegedly unpatentable based on the teachings of *Hayes , Hotchkiss, Behun, Nishikawa, et al.* and *Denning, et al.*, and further in view of *Okumura.*

As discussed above, *Hayes , Hotchkiss, Behun, Nishikawa, et al.* and *Denning, et al.* fails to disclose or suggest Appellant's claimed method that includes forming a metal ball bump having a eutectic layer formed thereon, with the eutectic layer mounted to a mounting board.

Referring to *Okumura* Figure 6b, *Okumura* teaches contacting opposing metal ball bumps 8 and 23 directly to one another, with no eutectic solder layer formed on either metal ball bump 8 or 23.

Therefore, *Hayes, Hotchkiss, Behun, Nishikawa,* and *Denning* and further in view of *Okumura* still fails to disclose or suggest Applicant's claim 7.

Claims 14 and 15 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Appellants respectfully request that the Board reverse the rejection.

C. **Claim 18 is not unpatentable under 35 U.S.C. §103(a) based on the teachings of *Hayes, Hotchkiss, Behun* and further in view of *Jackson***

Appellant respectfully submits that the Examiner's assertions are incorrect as a matter of fact and law. Thus, for the reasons set forth below, Appellant respectfully requests that

this Board reverse the rejection of claim 18 under 35 U.S.C. §103(a) as being allegedly unpatentable based on the teachings of *Hayes*, *Hotchkiss, Behun* and further in view of *Jackson.*

As discussed above, *Hayes*, *Hotchkiss,* and *Behun* fails to disclose or suggest Appellant's claimed method that includes forming a metal ball bump having a eutectic layer formed thereon, with the eutectic layer mounted to a mounting board.

Jackson fails to even mention metal ball bumps or forming eutectic solder layers on metal ball bumps.

Therefore, *Hayes, Hotchkiss, Behun* and further in view of *Jackson* still fails to disclose or suggest Applicant's claim 7.

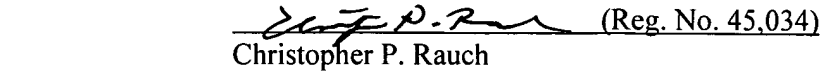
Claim 18 depends directly or indirectly from claim 7 and is therefore allowable for at least the same reasons that claim 7 is allowable.

Appellants respectfully request that the Board reverse the rejection.

VIII. CONCLUSION:

For the foregoing reasons, Appellants respectfully submit that the rejections posed by the Examiner are improper as a matter of law and fact. Accordingly, Appellants respectfully request the Board reverse the rejections of claims 7, 8, and 10-21.

Respectfully submitted,



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CLAIMS APPENDIX

Claim 7. A method of producing a semiconductor apparatus, the method comprising the steps of:

forming metal ball bumps in direct contact with a circuit pattern of a semiconductor device formed on a semiconductor substrate in a semiconductor wafer state;

forming a resin film on a circuit pattern forming surface of said semiconductor device so as to seal spaces between said metal ball bumps and to become thinner than a height of the metal ball bumps;

cleaning the surfaces of the metal ball bumps projecting out from the resin film;

after the cleaning step, forming eutectic solder layers different in composition from the metal ball bumps on the surfaces of the metal ball bumps;

after the forming solder layers step, cutting the semiconductor substrate into unit semiconductor chips, each semiconductor chip having at least one of said semiconductor device; and

after the cutting step, mounting at least one of the semiconductor chips on a mounting board from a bump forming surface side of the semiconductor chip so as to connect the eutectic solder layers of the semiconductor chip to the mounting board with the resin film directly contacting the semiconductor chip and not directly contacting the mounting board.

Claim 8. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface.

Claim 10. A process of production of the semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, any resin film components deposited on said bumps are removed.

Claim 11. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, oxides on said bump surfaces are removed.

Claim 12. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed by plasma cleaning.

Claim 13. A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least sputter etching by discharge plasma of an inert gas.

Claim 14. A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of an inert gas.

Claim 15. A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of a reducing gas.

Claim 16. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed by irradiating a laser beam.

Claim 17. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

Claim 18. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed while applying a gas jet to the bumps to peel off the unnecessary components which are then sucked away.

Claim 19. A process of production of a semiconductor apparatus as set forth in claim 7, wherein

the metal ball bumps formed in the first step are solder bumps.

Claim 20. A process of production of a semiconductor apparatus as set forth in claim 19, wherein said solder bumps have a melting point higher than a melting point of said eutectic solder layers and said eutectic solder layers are comprised of a eutectic solder.

Claim 21. A process of production of a semiconductor apparatus as set forth in claim 20, wherein, in said forming solder layers step, the eutectic solder layers are formed by a printing method, plating method, or transfer method.

EVIDENCE APPENDIX

Appellants do not submit extraneous evidence with this Main Brief on Appeal.

RELATED PROCEEDINGS APPENDIX

Appellants are not aware of any related appeals or interferences with regard to the present application.